ELECTRONICS & COMMUNICATION ENGINEERING

1. Analog & Digital Electronics and Circuits

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1. Assertion (A): In avalanche breakdown, the reverse current sharply increases with voltage due to a field emission.

Reason (R): The field, emission requires highly doped p and n regions.

- **A)** Both A and R are true and R is the correct explanation of A
- **B)** Both A and R are true but R is NOT the correct explanation of A
- C) A is true but R is false
- **D)** A is false but R is true
- Assertion (A): In small signal class 'A' amplifier, the output is a magnified replica of the input without any change in frequency. Reason (R): The dc operating point is fixed in class 'A' position.
 - **A)** Both A and R are true and R is the correct explanation of A
 - **B)** Both A and R are true but R is NOT the correct explanation of A
 - C) A is true but R is false
 - **D)** A is false but R is true
- 3. Assertion (A): D-latch and edge-triggered D-flip flop (FF are functionally different. Reason (R): In D-latch the output (O) can change while enable (EN) is high. In D-FF the output can change only on the active edge of CLK.
 - A) Both A and R are true and R is the correct explanation of A
 - **B)** Both A and R are true but R is NOT the correct explanation of A
 - C) A is true but R is false
 - **D)** A is false but R is true
- 4. Assertion (A): D-flip flops are used to construct a buffer register. Reason (R): Buffer registers are used to store
 - a binary word temporarily.
 - 1. (D) 2. (C) 3. (A)

- A) Both A and R are true and R is the correct explanation of A
- **B)** Both A and R are true but R is NOT the correct explanation of A
- **C)** A is true but R is false

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- **D)** A is false but R is true
- Assertion (A): Linear AM detector applied with two amplitude-modulated waves simultaneously, one being very weak with respect to the other, detects only the strong signal. Reason (R): Detector selectivity is increased in the presence of strong signal.
 - A) Both A and R are true and R is the correct explanation of A
 - **B)** Both A and R are true but R is NOT the correct explanation of A
 - **C)** A is true but R is false
 - **D)** A is false but R is true
- Assertion (A): Coherent FSK system is preferred over non-coherent FSK.

Reason (R): Coherent FSK requires less power than non-coherent FSK.

- A) Both A and R are true and R is the correct explanation of A
- **B)** Both A and R are true but R is NOT the correct explanation of A
- C) A is true but R is false
- **D)** A is false but R is true
- 7. Assertion (A): High frequency power supplies are light weight.

Reason (R): Transformer size get reduced at high frequency.

- **A)** Both A and R are true and R is the correct explanation of A
- **B)** Both A and R are true but R is NOT the correct explanation of A
- $\textbf{C)} \quad A \text{ is true but } R \text{ is false}$
- $\textbf{D} \textbf{)} \hspace{0.1in} A \hspace{0.1in} \text{is false but } R \hspace{0.1in} \text{is true} \\$

7. (B)

3. (A) 4. (A) 5. (D)



6. (B)

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- 8. A specimen of intrinsic germanium with the density of charge carries of 2.5×10^{13} /cm³, is doped with donor impurity atoms such that there is one donor impurity atom for ever 10^6 germanium atoms. The density of germanium atoms is 4.4×10^{22} /cm³. The hole density would be
 - **A)** $4.4 \times 10^{16} / \text{ cm}^3$
 - **B)** 1.4×10^{10} / cm³
 - **C)** 4.4×10^{10} / cm³
 - **D)** 1.4×10^{16} / cm³
- 9. In a forward biased photo diode, an increase in incident light intensity causes' the diode current to
 - A) Increase B) Remain constant
 - C) Decrease
 - **D)** Remain constant while the voltage drop across the diode increases
- 10. If for intrinsic Silicon at 27° C, the charge concentration and mobilities of free electrons and holes are 1.5×10^{16} per m³, $0.13m^2/(Vs)$ and $0.05 m^2/(Vs)$ respectively, its conductivity will be
 - **A)** 2.4×10^{-3} (Ω -m)⁻¹
 - **B)** 3.15×10^{-3} (Ω -m)⁻¹
 - **C)** $5 \times 10^{-4} (\Omega m)^{-1}$
 - **D)** 4.32×10^{-4} (Ω -m)⁻¹
- 11.



A circuit using the .BJT is shown in the above figure, the value of β is

- A)
 120
 B)
 150

 C)
 165
 D)
 166
- 12. Bridge rectifiers are preferred becauseA) They require small transformer
 - B) They have less peak inverse voltage
 - **C)** They need small transformer and also
 - have less peak inverse voltage
 - **D)** They have low ripple factor



For the circuit shown in the above figure h_{11} ,

- $\mathbf{h}_{_{12}},\,\mathbf{h}_{_{21}}$ and $\mathbf{h}_{_{22}}$ are respectively
- **A)** 0.5, 0.5, 0.125 and 6
- **B)** 6, 0.5, 0.5 and 0.125
- **C)** 0.5, 0.5, 6 and 0.125
- **D)** 0.125, 6, 0.5 and 0.5
- 14. In an RC coupled amplifier, the gain decreases in the frequency response due to the
 - A) Coupling capacitor at low frequency and bypass capacitor at high frequency
 - **B)** Coupling capacitor at high frequency arid bypass capacitor at low frequency
 - C) Coupling junction capacitance at low frequency and coupling capacitor at high frequency
 - D) Device junction capacitor at high frequency and coupling capacitor at low frequency
- 15. The Darlington pair has a current gain of approximately β^{2} , the voltage gain AV, the input resistance Ri and the output resistance R_{0} . when the Darlington pair is used in the emitter follower configuration, A_{v} , R_{i} and R_{0} are respectively
 - A) Very large, very large and very small
 - B) Unity, very large and very small
 - C) Unity, very small and very large
 - D) Very large, very small and very large

8. (D) 9. (D) 10. (D) 11. (C) 12. (C) 13. (B) 14. (D) 15. (B)

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16.	Match List I with List II and select the correct answer: List I a. h _{ie} b. h _{fe} c. h _{re} d. h _{oe} List II (Units/delimitations)						 19. "Slope overload" occurs in delta modulation when the A) Frequency of the clock pulses is too low B) Rate of change of analog waveform is too large C) Step size is too small D) Analog signal varies very slowly with time 	
	1. Cu 2. Oh 3. Sie 4. Vo Code A) B) C) D)	rrrent ams emen ltage s: a) 2 1 1 2	t tra s tra b) 1 2 2 1	nsfe nsfe c) 3 4 3 4	r ratio d) 4 3 4 3	20.	The slew rate of an op-amp is 0.5V/micro sec. The maximum frequency of a sinusoidal input of 2 V rms that can be handled without excessive distortion is A) 3kHz B) 30kHz C) 200kHz D) 2MHz V _S O V _S O V _S O V _S O V _S O V _S O V _S O	
17.	An au $4 \Omega g$ 6 V (i) deliv A) 1 C) 2 Input For t $\beta = 1$ be in A) C B) In C) A D) S	mplif gives rms). er to .5 W .4 W 	ier l an Th a lo rcui or th f req se ac e reg ation	avi ope e ma bad i 20 20 20 20 20 20 20 20 20 20 20 20 20	ng an output resistance of n circuit output voltage of aximum power that it can s B) 2.25 W D) 9 W	22.	An op-amp is used in the circuit as shown in the above figure. Current I_0 is A) $V_s \times \frac{R_L}{R_S(R_L + R_S)}$ B) $V_s R_s$ C) $V_s R_L$ D) $V_s \left(\frac{1}{R_S} + \frac{1}{R_L}\right)$ A circuit with op-amp is shown in the above figure. The voltage V_0 is A) $3Vs_1 - 6Vs_2$ B) $2Vs_1 - 3Vs_2$ C) $2Vs_1 - 2Vs_2$ D) $3Vs_1 - 2Vs_2$	
1	6. (A)	17	. (D))	18. (D) 19. (C) 20. (B)	21.	(B) 22. (D)	
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27.

- 23. A sinusoidal waveform can be converted to a square waveform by using a
 - A) Two stage transistorized over driven amplifier
 - B) Two stage diode detector circuit
 - **C)** Voltage comparator based on op-amp
 - **D)** Regenerative voltage comparator circuit



For the circuit shown in the above figure, by assuming $\beta = 200$ and $V_{\rm BE} = 0.7$ V, the best approximation for the collector current Ic in the active region is

- **A)** 1 mA **B)** 2.4 mA
- **C)** 3 mA **D)** 9.6 mA
- 25. High power efficiency of the push-pull amplifier is due to the face that
 - A) Each transistor conducts on different cycle of the input
 - B) Transistors are placed in CE configuration
 - **C)** There is no quiescent collector current
 - **D)** Low forward biasing voltage is required









The Schmitt trigger circuit is shown in the above figure. If $V_{sat} = \pm 10$ V, the tripping point for the increasing input voltage will be

A)	1 V	B) 0.893 V
0	0 47757	$\mathbf{D} = 0.416 \mathbf{V}$

0	0.477V	D) 0.410V

28. In Boolean Algebra, If $F = (A + B)(\overline{A} + C)$, then

A)
$$F = AB + AC$$
 B) $F = AB + \overline{AB}$
C) $F = AC + \overline{A}B$ D) $F = AA + \overline{A}B$

29.



A switch circuit using the transistor is shown in the above figure. Assume hFE(min) = 20 and f τ = 100MHz. The most dominant speed limitation is brought by

A)	Rise time	B) Fall time
C)	Storage time	D) Delay time

28. (C)

29. (A)